

***PROBLEM STATEMENT***

**Day 1** : Simple Wire

**Day 2** : Four Wires

**Day 3** : Inverter

**Day 4** : And Gate

**Day 5** : Nor Gate

**Day 6** : Xnor Gate

**Day 7** : Declaring Wires

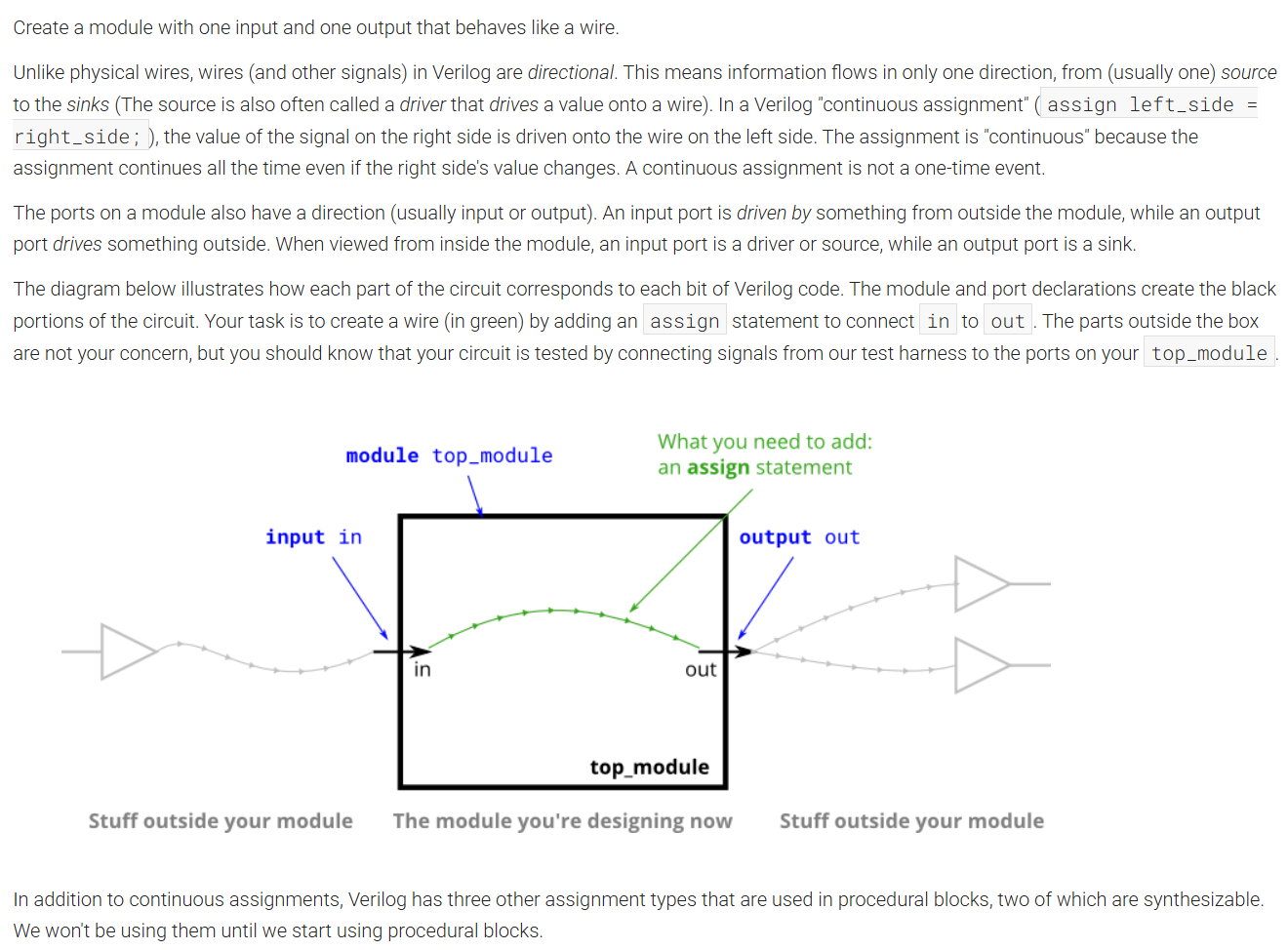
**Day 8** : 7458 Chip

**Day 9** : Vectors

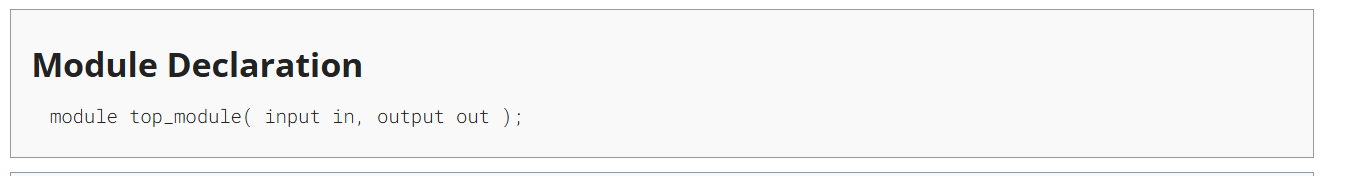
**Day 10** : Declaring Vectors

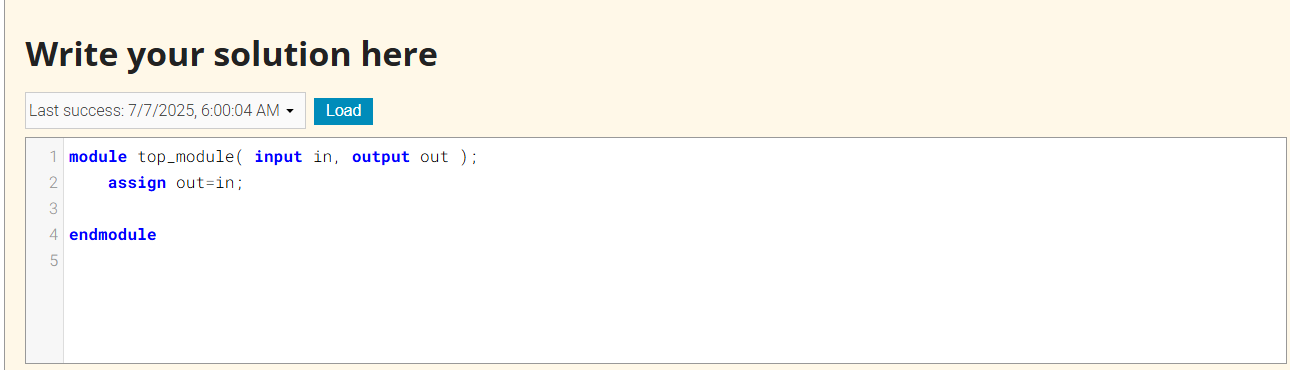
**DAY:1**

**Problem Statement:**



**Module Declaration:**

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**Solution: **

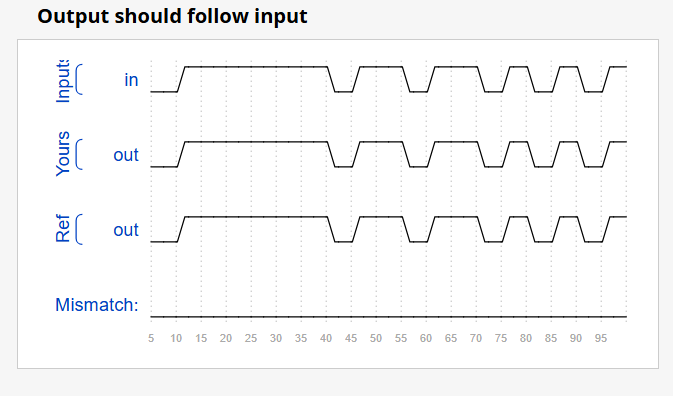
**Code:**

module top\_module( input in, output out );

assign out=in;

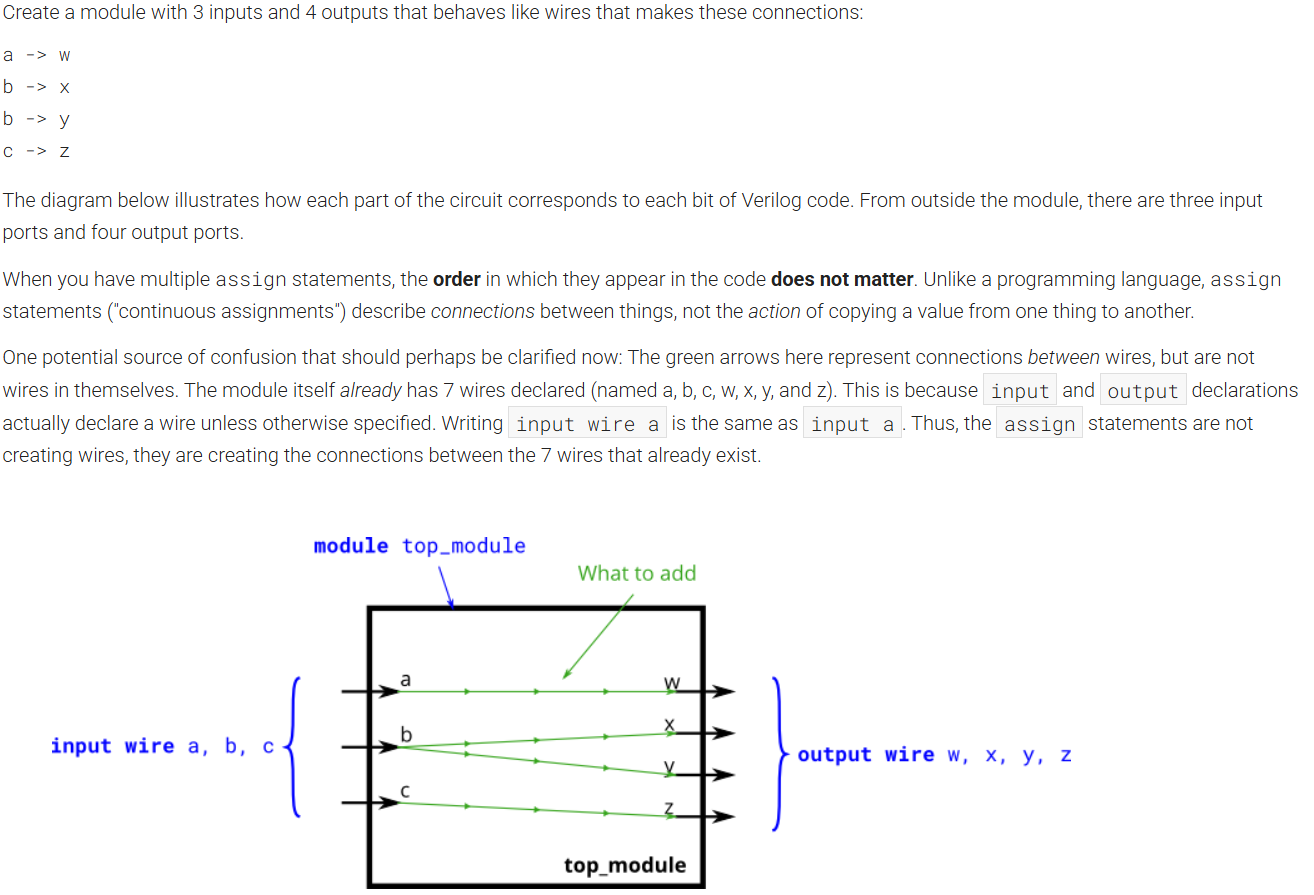
endmodule

**Timing Diagram:**

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**DAY:2**

**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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**Code:**

module top\_module (

input a,

input b,

input c,

output w,output x, output y, output z );

assign w = a;

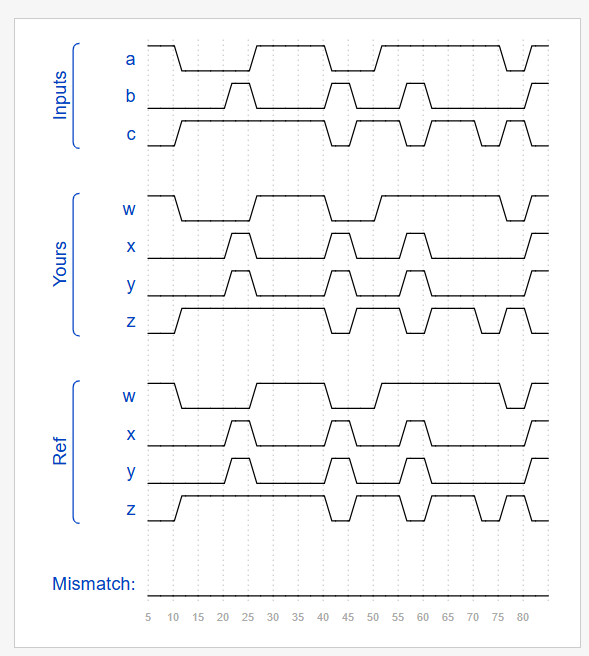
assign x = b;

assign y = b;

assign z = c;

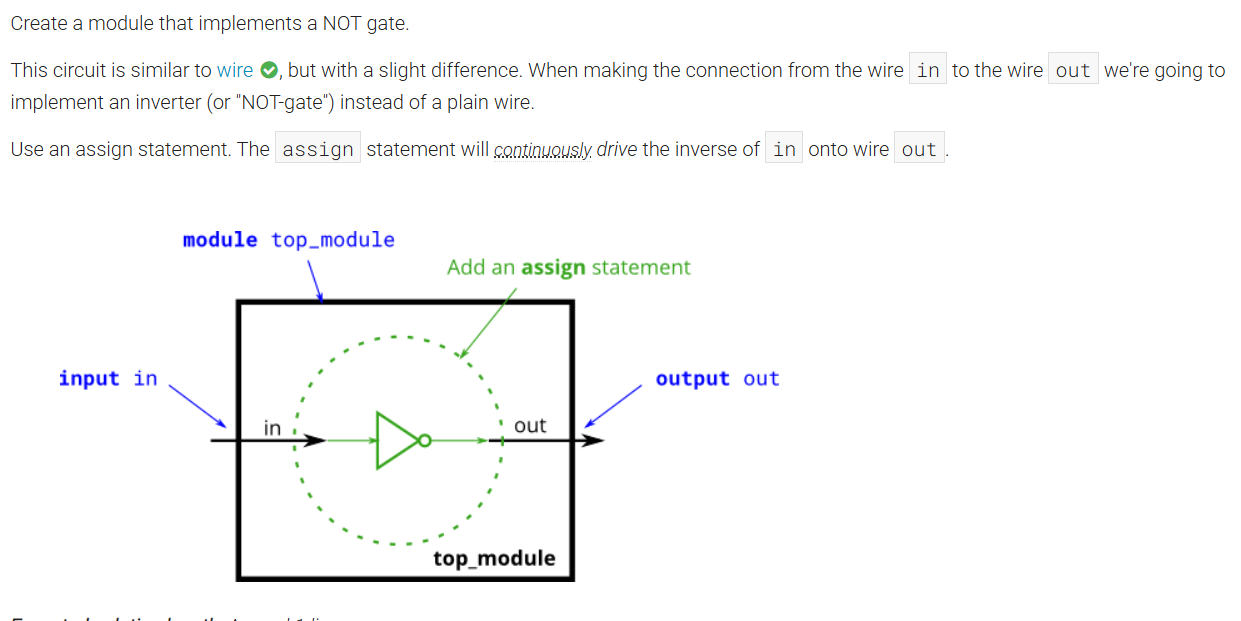
endmodule

**Timing Diagram:**



**DAY:3**

**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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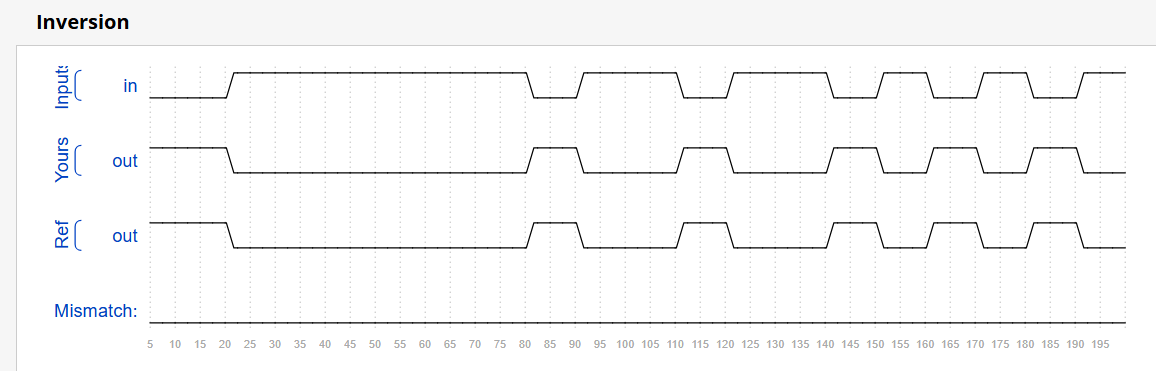
**Code:**

module top\_module( input in, output out );

assign out=~in;

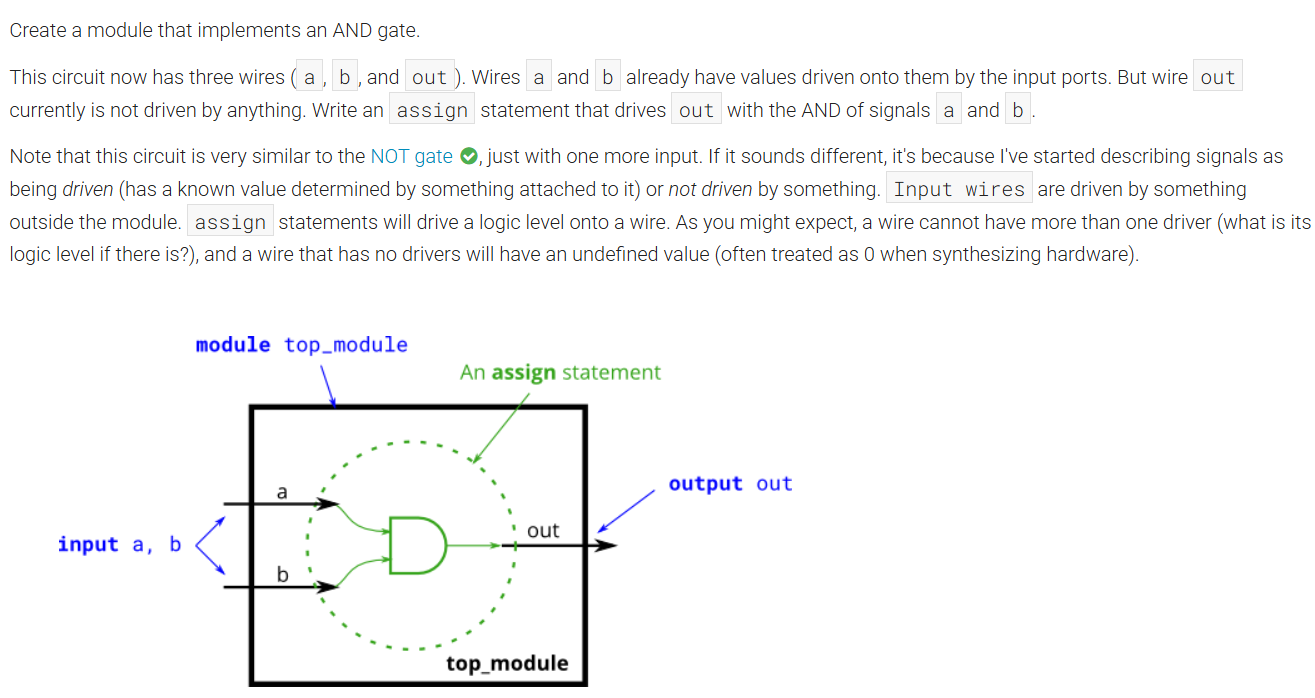
endmodule

**Timing Diagram:**

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**DAY:4**

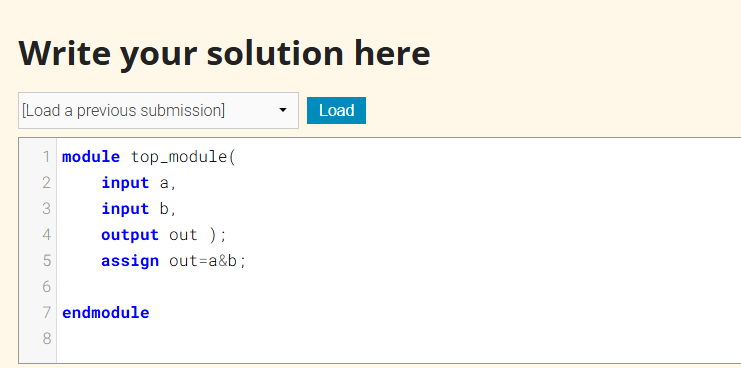
**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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**Code:**

module top\_module(

input a,

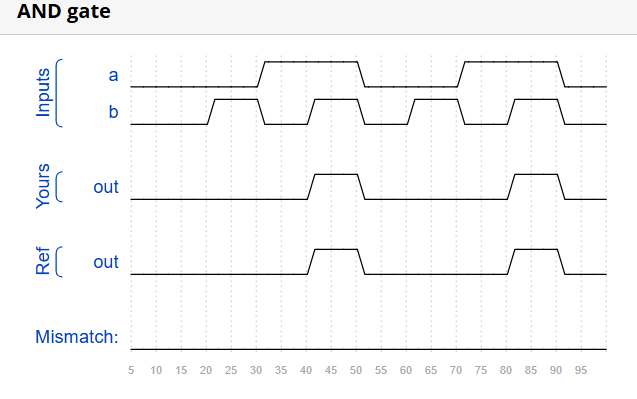
input b,

output out );

assign out=a&b;

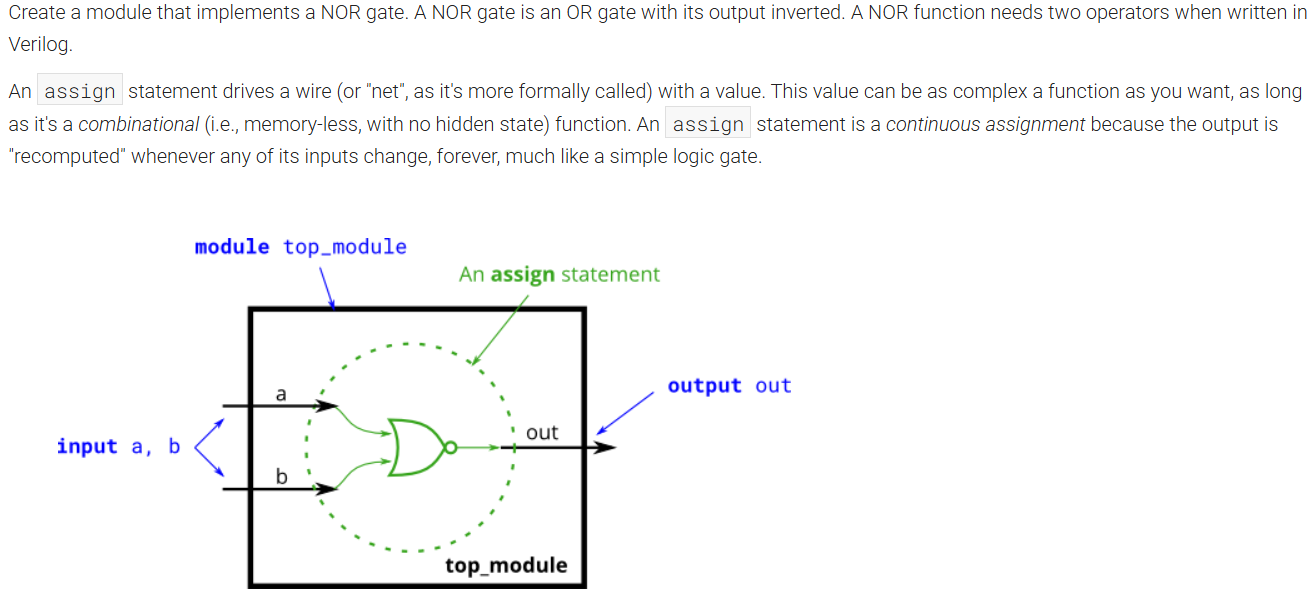
endmodule

**Timing Diagram:**

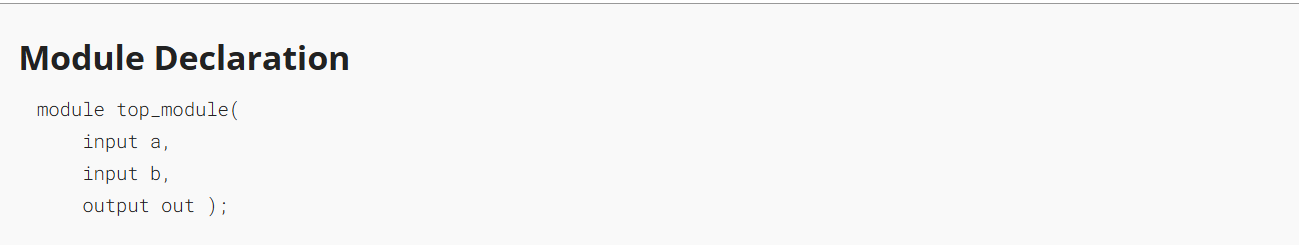
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**DAY:5**

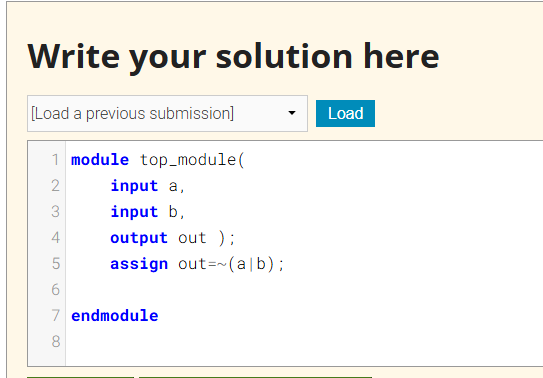
**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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**Code:**

module top\_module(

input a,

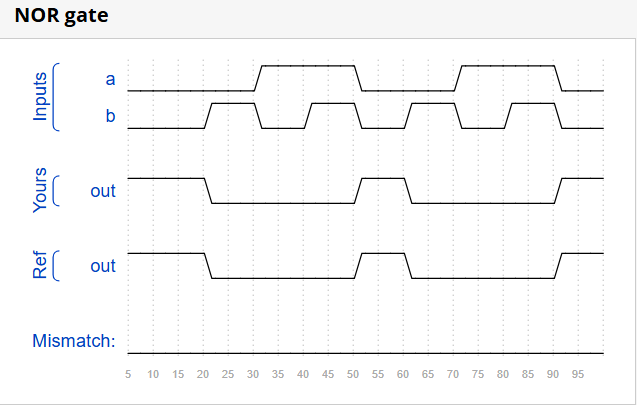
input b,

output out );

assign out=~(a|b);

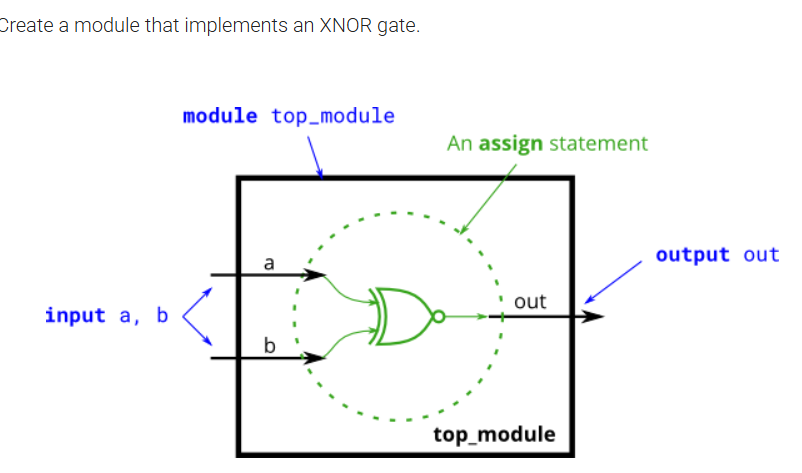
endmodule

**Timing Diagram:**

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**DAY:6**

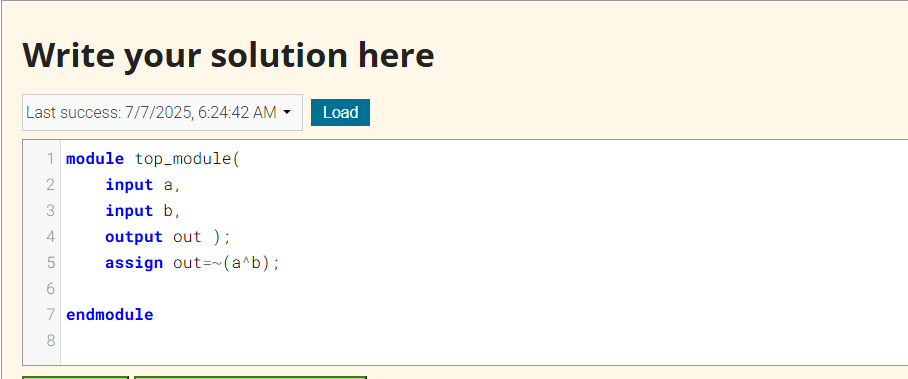
**Problem Statement:**

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**Module Declaration:**

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**Solution:**



**Code:**

module top\_module(

input a,

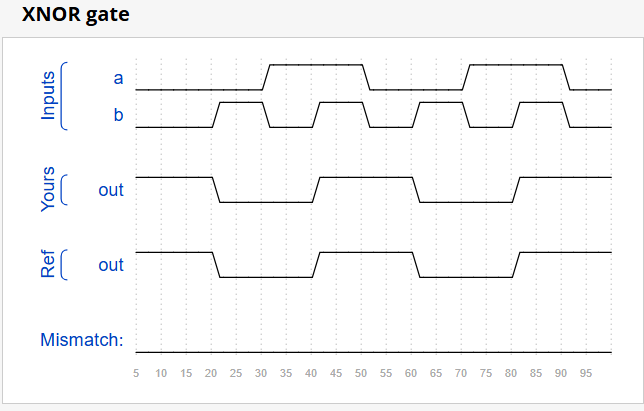
input b,

output out );

assign out=~(a^b);

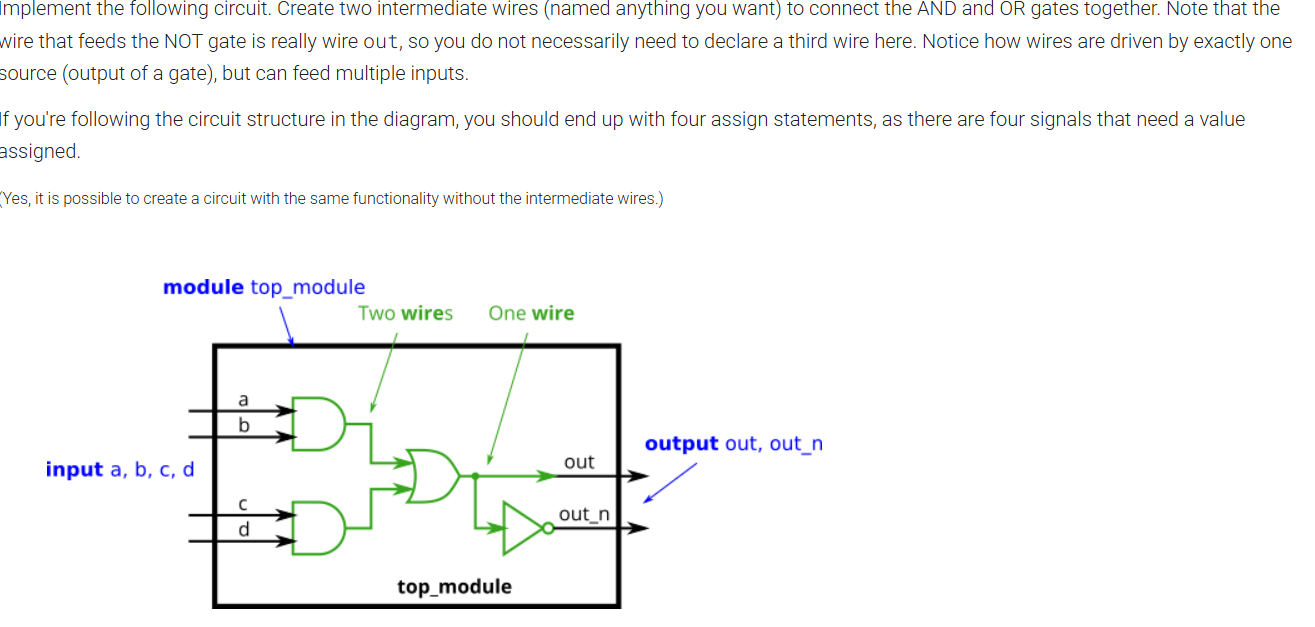
endmodule

**Timing Diagram:**

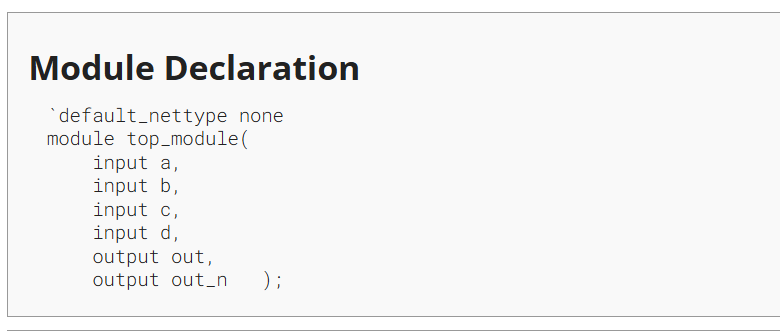
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**DAY:7**

**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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**Code:**

module top\_module(

input a,

input b,

input c,

input d,

output out,

output out\_n );

wire x,y,z;

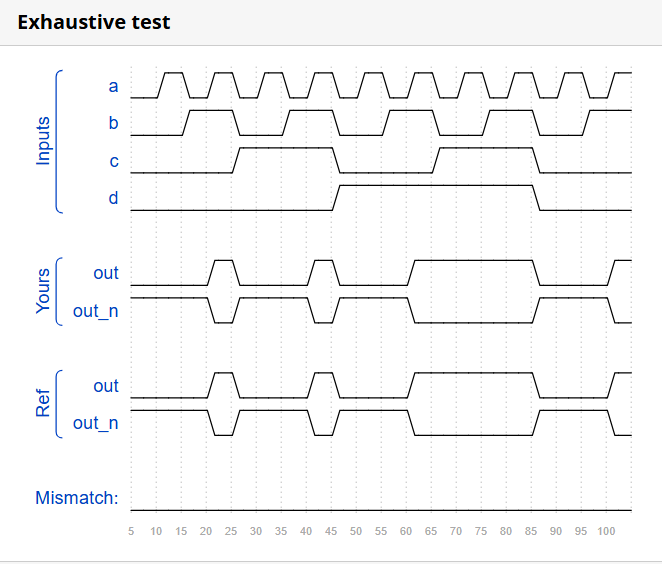
assign x=(a&b);

assign y=(c&d);

assign out=(x|y);

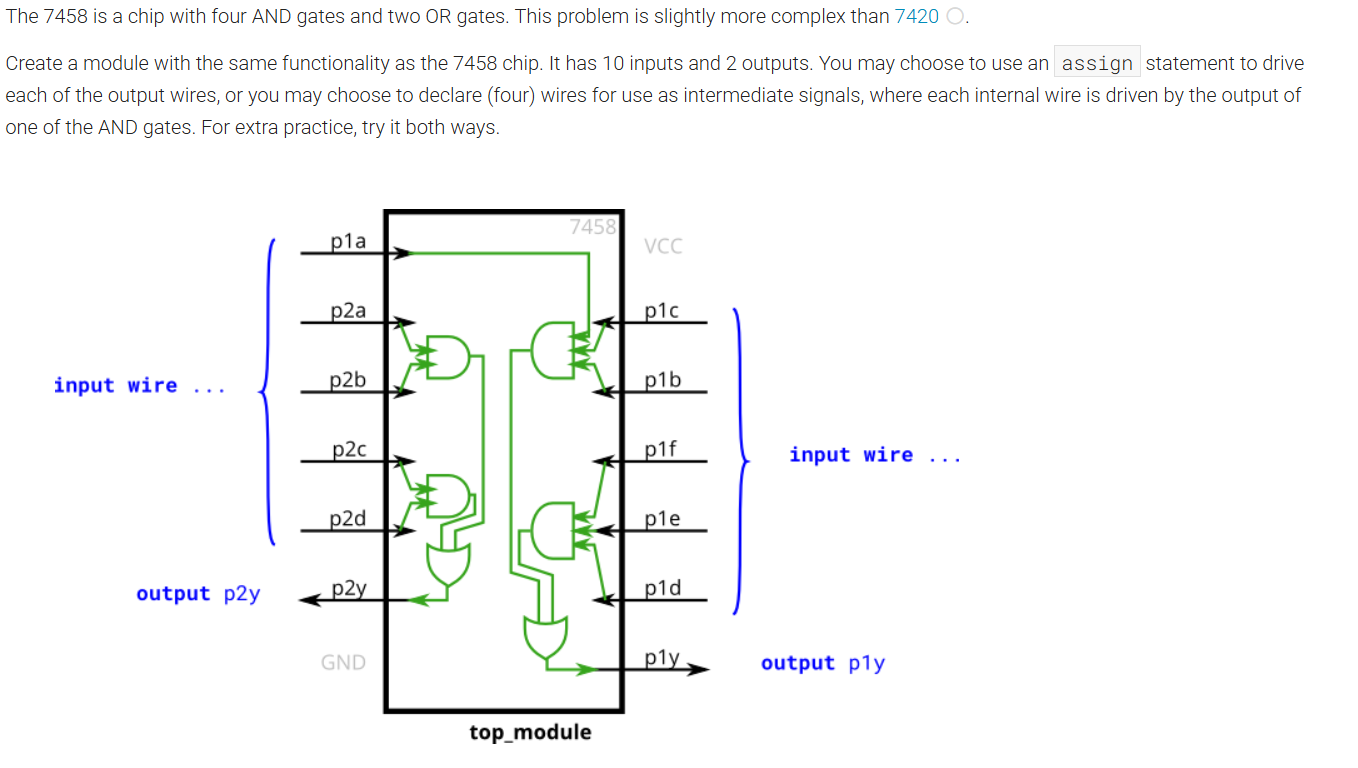
assign out\_n=~(x|y);

endmodule

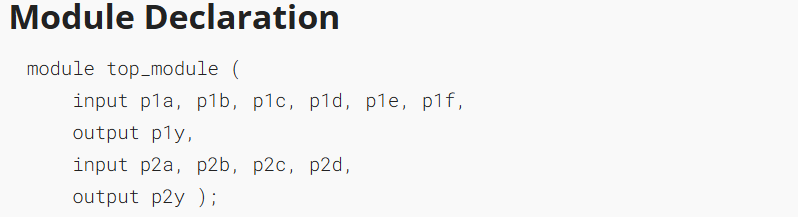
**Timing Diagram:**

**DAY:8**

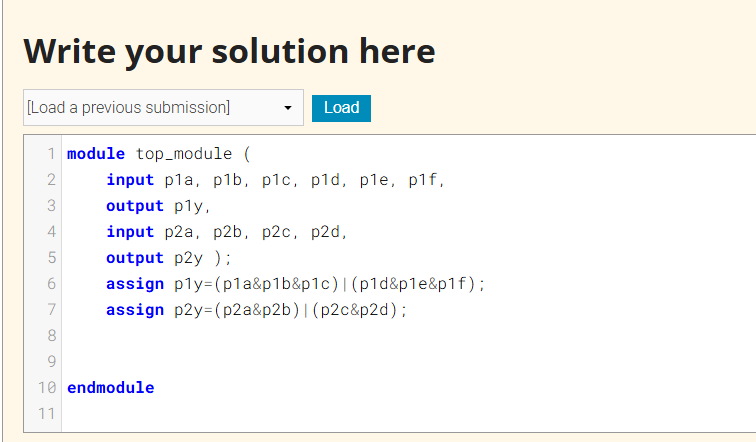
**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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**Code:**

module top\_module (

input p1a, p1b, p1c, p1d, p1e, p1f,

output p1y,

input p2a, p2b, p2c, p2d,

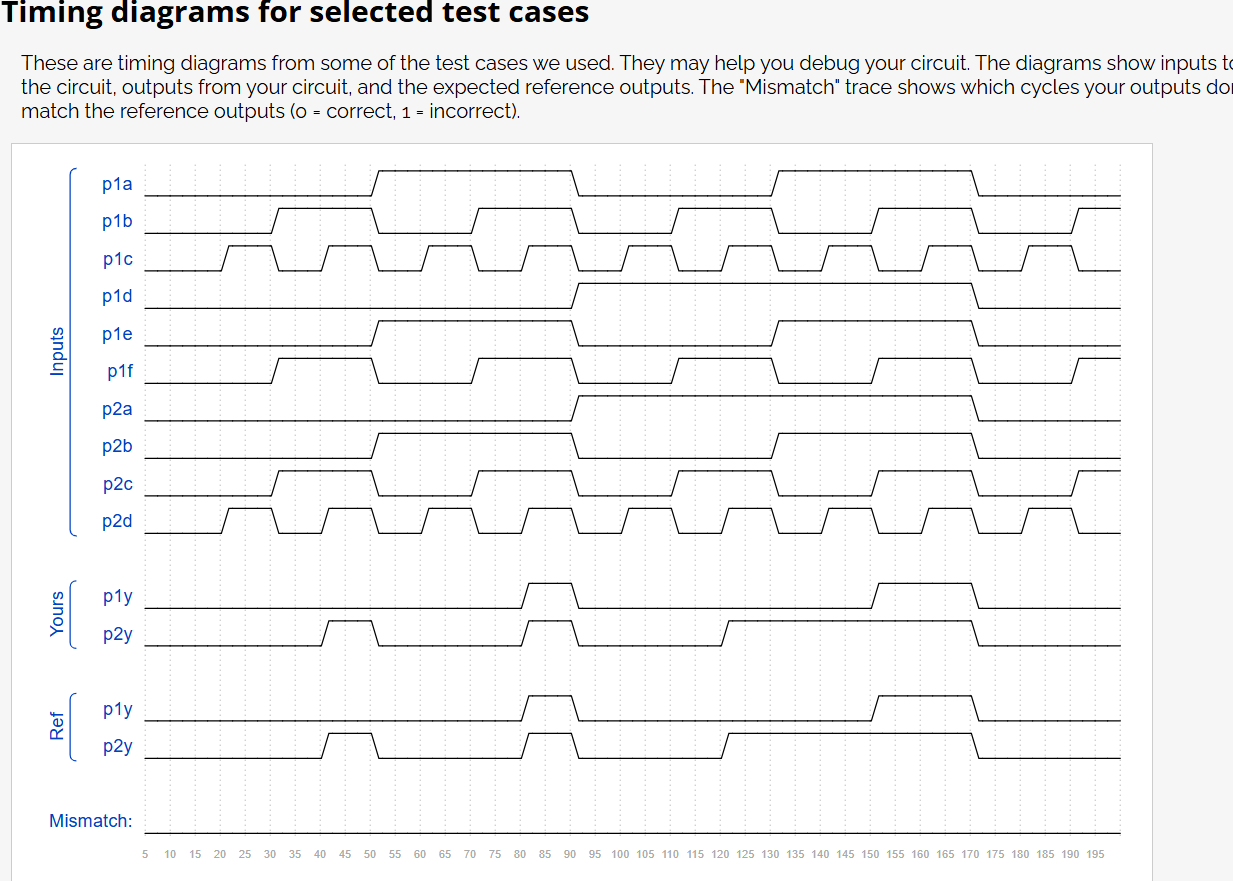
output p2y );

assign p1y=(p1a&p1b&p1c)|(p1d&p1e&p1f);

assign p2y=(p2a&p2b)|(p2c&p2d);

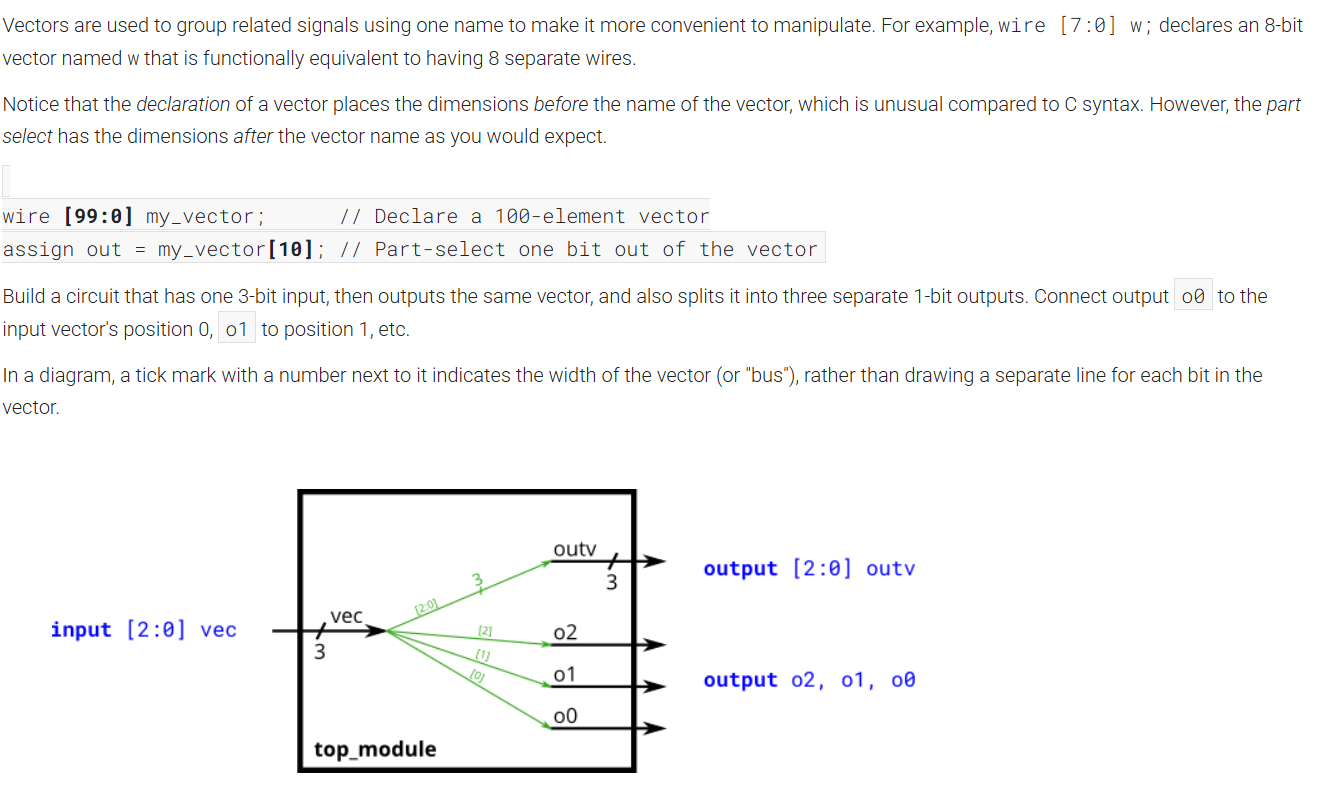
endmodule

**Timing Diagram:**

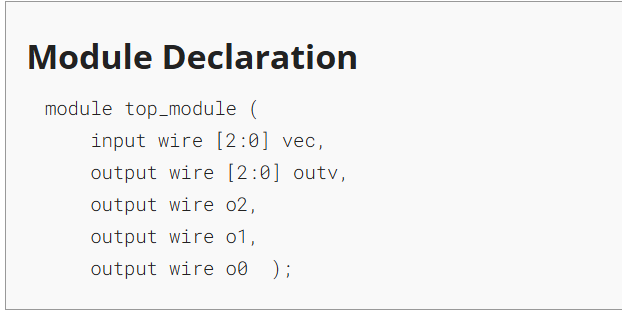


**DAY:9**

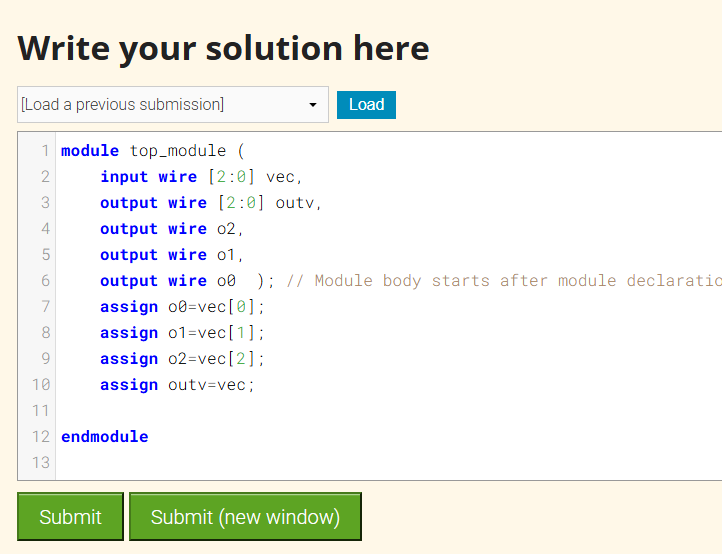
**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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**Code:**

module top\_module (

input wire [2:0] vec,

output wire [2:0] outv,

output wire o2,

output wire o1,

output wire o0 );

assign o0=vec[0];

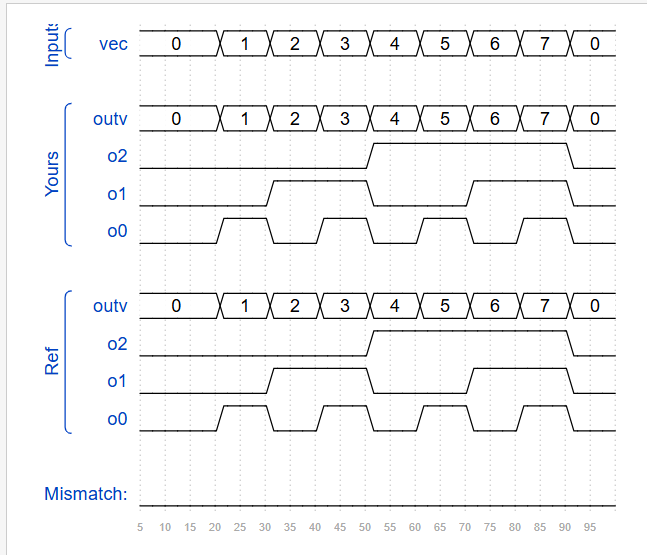
assign o1=vec[1];

assign o2=vec[2];

assign outv=vec;

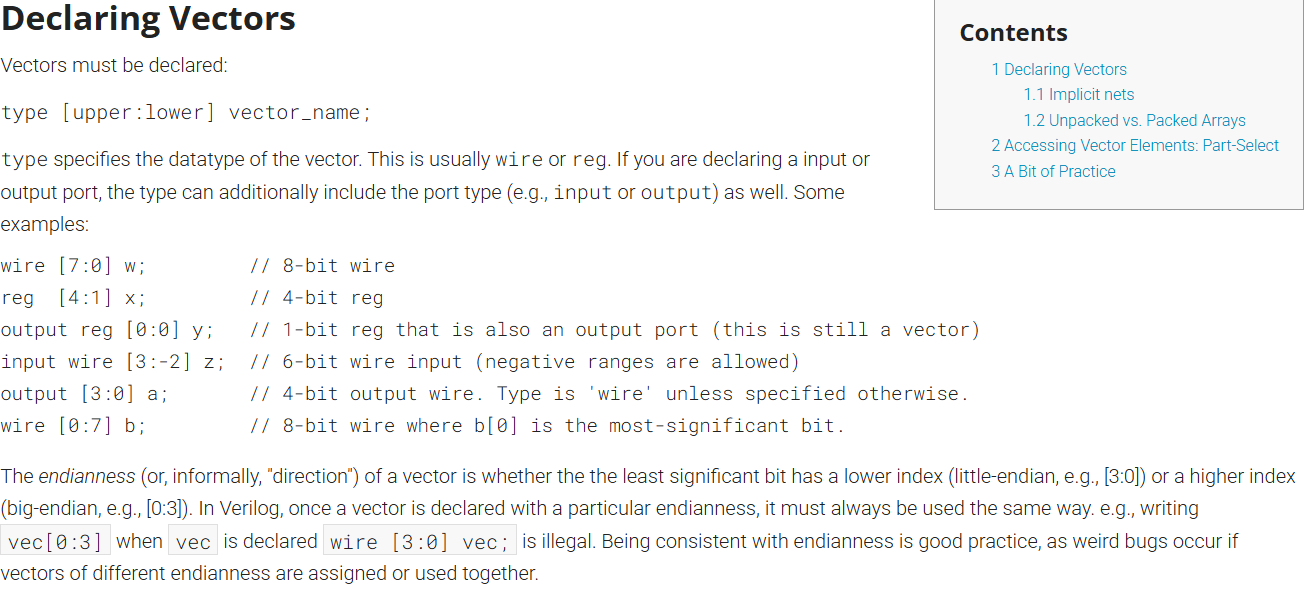
endmodule

**Timing Diagram:**

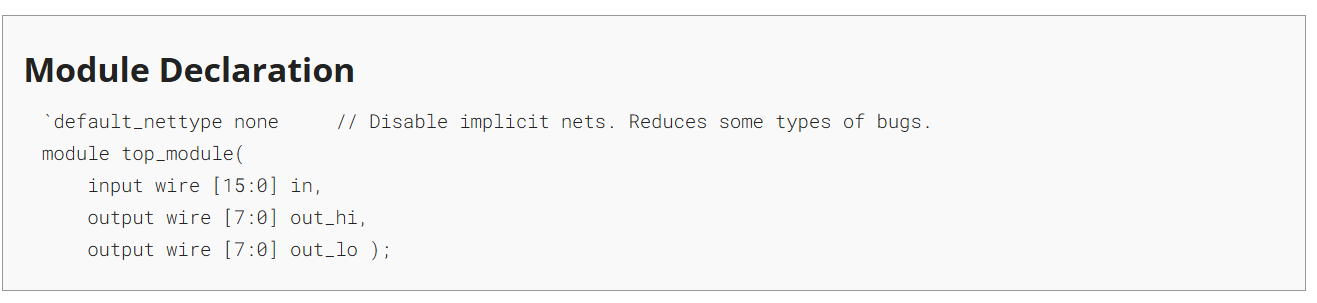
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**DAY:10**

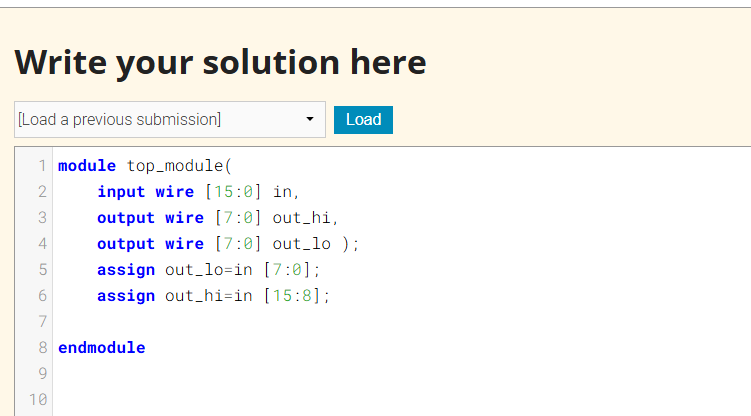
**Problem Statement:**

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**Module Declaration:**

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**Solution:**

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**Code:**

module top\_module(

input wire [15:0] in,

output wire [7:0] out\_hi,

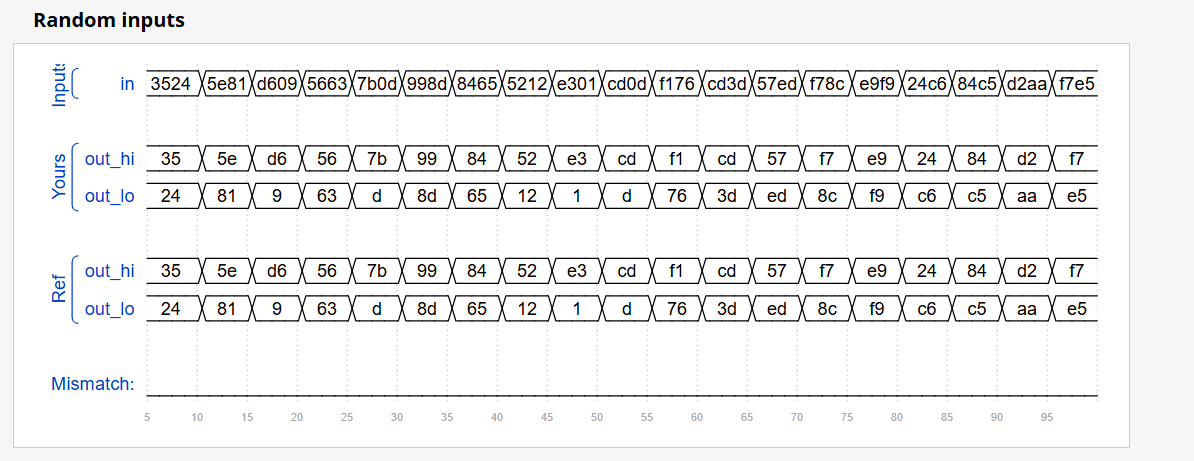
output wire [7:0] out\_lo );

assign out\_lo=in [7:0];

assign out\_hi=in [15:8];

endmodule

**Timing Diagram:**

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